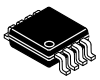
P2040A

Product Preview

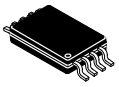
LCD Panel EMI Reduction IC

ON Semiconductor®

http://onsemi.com

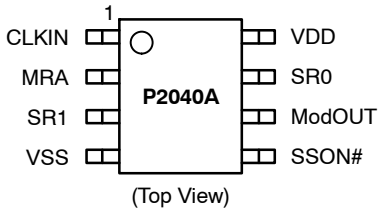


SOIC−8
S SUFFIX
CASE 751BD



TSSOP−8
T SUFFIX
CASE 948AL

PIN CONFIGURATION



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

Product Description

The P2040A is a versatile spread spectrum frequency modulator designed specifically for digital flat panel applications. The P2040A reduces electromagnetic interference (EMI) at the clock source, allowing system wide reduction of EMI of down stream clock and data dependent signals. The P2040A allows significant system cost savings by reducing the number of circuit board layers, ferrite beads, shielding, and other passive components that are traditionally required to pass EMI regulations.

The P2040A uses the most efficient and optimized modulation profile approved by the FCC and is implemented in a proprietary all digital method.

The P2040A modulates the output of a single PLL in order to "spread" the bandwidth of a synthesized clock, and more importantly, decreases the peak amplitudes of its harmonics. This results in significantly lower system EMI compared to the typical narrow band signal produced by oscillators and most frequency generators. Lowering EMI by increasing a signal's bandwidth is called 'spread spectrum clock generation.'

Features

- FCC Approved Method of EMI Attenuation
- Provides up to 20 dB of EMI Suppression
- Generates a Low EMI Spread Spectrum Clock of the Input Frequency
- Input Frequency Range: 30 MHz to 100 MHz
- 3.3 V Operating Voltage
- Optimized for VGA, SVGA, and Higher Resolution XGA LCD Panels
- Internal Loop Filter Minimizes External Components and Board Space
- Six Selectable High Spread Ranges up to ±2%
- Two Selectable Modulation Rates
- SSON# Control Pin for Spread Spectrum Enable and Disable Options
- Low Cycle−to−Cycle Jitter
- Wide Operating Range
- Low Power CMOS Design
- Supports Most Mobile Graphic Accelerator Specifications
- Products Available for Automotive Temperature Range. (Refer to *Spread Range Selection* Tables)
- Available in 8−pin SOIC and TSSOP Packages
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

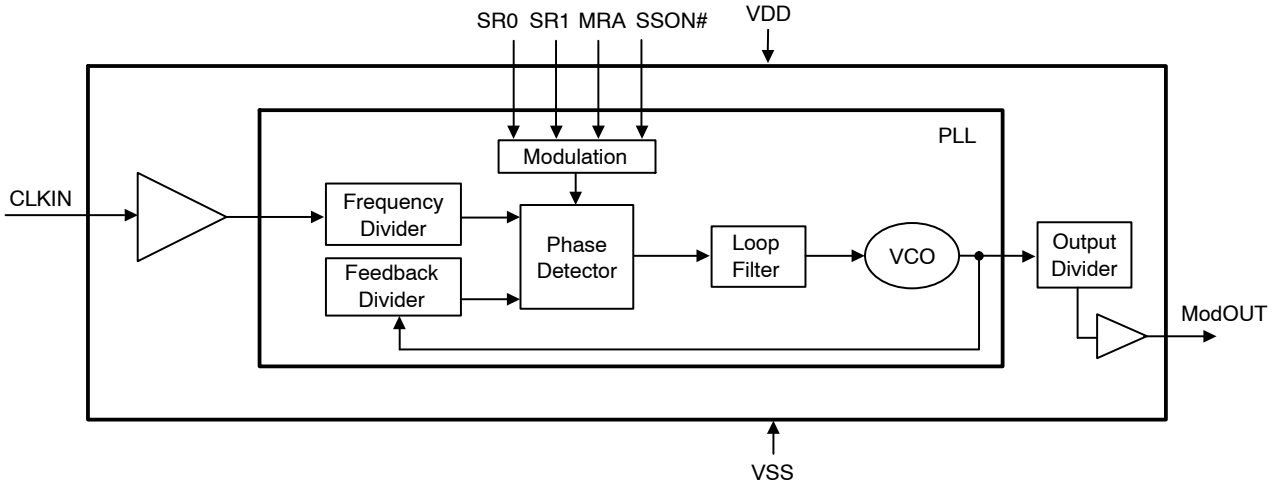


Figure 1. Block Diagram

Table 1. PIN DESCRIPTION

Pin#	Pin Name	Type	Description
1	CLKIN	I	External reference frequency input. Connect to externally generated reference signal.
2	MRA	I	Digital logic input used to select modulation rate. This pin has an internal pull−up resistor.
3	SR1	I	Digital logic input used to select Spreading Range. This pin has an internal pull−up resistor.
4	VSS	P	Ground to entire chip. Connect to system ground.
5	SSON#	I	Digital logic input used to enable Spread Spectrum function (Active LOW). Spread Spectrum function enabled when LOW, disabled when HIGH. This pin has an internal pull−low resistor.
6	ModOUT	O	Spread spectrum clock output.
7	SR0	I	Digital logic input used to select Spreading Range. This pin has an internal pull−up resistor.
8	VDD	P	Power supply for the entire chip (3.3 V).

Table 2. MODULATION SELECTION (Commercial)

MRA	SR1	SR0	Spreading Range	Modulation Rate (KHz)
0	0	0	±1.125	(FIN /40) * 34.72 KHz
0	0	1	±1.75	(FIN /40) * 34.72 KHz
0	1	0	±0.75	(FIN /40) * 34.72 KHz
0	1	1	±1.25	(FIN /40) * 34.72 KHz
1	0	0	±1.25	(FIN /40) * 20.83 KHz
1	0	1	±2.00	(FIN /40) * 20.83 KHz
1	1	0	Reserved	Reserved
1	1	1	Reserved	Reserved

Table 3. SPREAD RANGE SELECTION AT 50 MHz (Automotive)

MRA	SR1	SR0	Spreading Range	Modulation Rate
0	0	0	±1.25	(F_{IN}/40) * 34.72 KHz
0	0	1	±2.00	(F_{IN}/40) * 34.72 KHz
0	1	0	±1.00	(F_{IN}/40) * 34.72 KHz
0	1	1	±1.50	(F_{IN}/40) * 34.72 KHz
1	0	0	±1.25	(F_{IN}/40) * 20.83 KHz
1	0	1	±2.00	(F_{IN}/40) * 20.83 KHz
1	1	0	±1.25	(F_{IN}/40) * 20.83 KHz
1	1	1	±2.00	(F_{IN}/40) * 20.83 KHz

Table 4. SPREAD RANGE SELECTION AT 70 MHz (Automotive)

MRA	SR1	SR0	Spreading Range	Modulation Rate
0	0	0	±1.00	(F_{IN}/40) * 34.72 KHz
0	0	1	±1.50	(F_{IN}/40) * 34.72 KHz
0	1	0	±0.70	(F_{IN}/40) * 34.72 KHz
0	1	1	±1.00	(F_{IN}/40) * 34.72 KHz
1	0	0	±1.15	(F_{IN}/40) * 20.83 KHz
1	0	1	±2.00	(F_{IN}/40) * 20.83 KHz
1	1	0	±1.15	(F_{IN}/40) * 20.83 KHz
1	1	1	±1.75	(F_{IN}/40) * 20.83 KHz

Spread Spectrum Selection

The *Modulation Selection* Table defines the possible spread spectrum options. The optimal setting should minimize system EMI to the fullest without affecting system performance. The spreading is described as a percentage deviation of the center frequency. (Note: The center frequency is the frequency of the external reference input on CLKIN, pin1).

For example, P2040A is designed for high−resolution, flat panel applications and is able to support an XGA (1024 x 768) flat panel operating at 65 MHz (F_{IN}) clock speed. A spreading selection of MRA=0, SR1=1 and SR0=0 provides a percentage deviation of ±0.75% from F_{IN}. This results in the frequency on ModOUT being swept from 64.51 MHz to 65.49 MHz at a modulation rate of 56.24 KHz. Refer to *Modulation Selection* Table. The example in the following illustration is a common EMI reduction method for a notebook LCD panel and has already been implemented by most of the leading OEM and mobile graphic accelerator manufacturers.

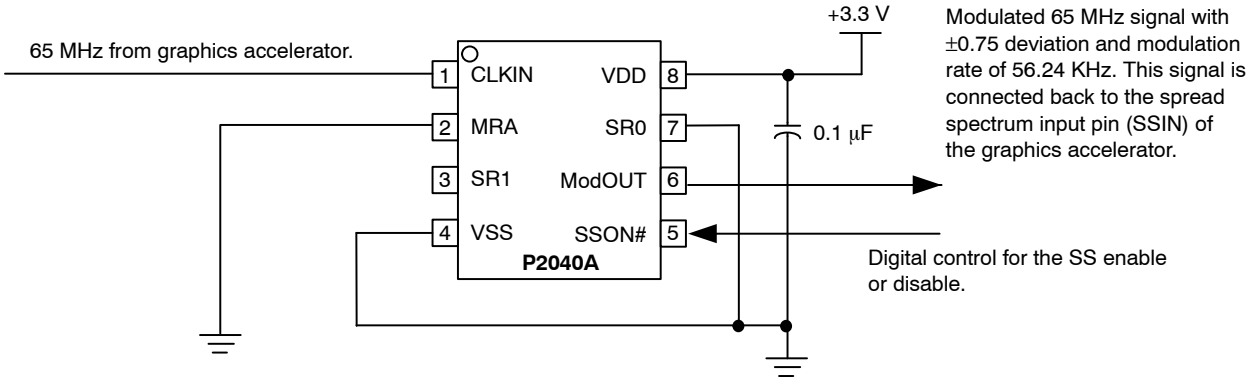


Figure 2. Application Schematic for Mobile LCD Graphics Controllers

Table 5. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Unit
VDD, V_{IN}	Voltage on any pin with respect to Ground	−0.5 to +4.6	V
T_{STG}	Storage temperature	−65 to +125	°C
T_A	Operating temperature	−40 to +125	°C
T_s	Max. Soldering Temperature (10 sec)	260	°C
T_J	Junction Temperature	150	°C
T_{DV}	Static Discharge Voltage (As per JEDEC STD22− A114−B)	2	KV

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 6. DC ELECTRICAL CHARACTERISTICS
(Test condition: All parameters are measured at room temperature (+25°C) unless otherwise stated.)

Symbol	Parameter	Min	Typ	Max	Unit
V_{IL}	Input low voltage	VSS−0.3	−	0.8	V
V_{IH}	Input high voltage	2.0	−	VDD+0.3	V
I_{IL}	Input low current (pull−up resistor on inputs SR0, SR1 and MRA)	−35	−	−	μA
I_{IH}	Input high current (pull−down resistor on input SSON#)	−	−	35	μA
V_{OL}	Output low voltage (VDD = 3.3 V, I_{OL} = 20 mA)	−	−	0.4	V
V_{OH}	Output high voltage (VDD = 3.3 V, I_{OH} = 20 mA)	2.5	−	−	V
I_{DD}	Static supply current standby mode	−	0.6	−	mA
I_{CC}	Dynamic supply current (3.3 V and 10 pF loading)	7	10	13	mA
VDD	Operating voltage	2.7	3.3	3.7	V
t_{ON}	Power−up time (first locked cycle after power up)	−	0.18	−	mS
Z_{OUT}	Clock output impedance	−	50	−	Ω

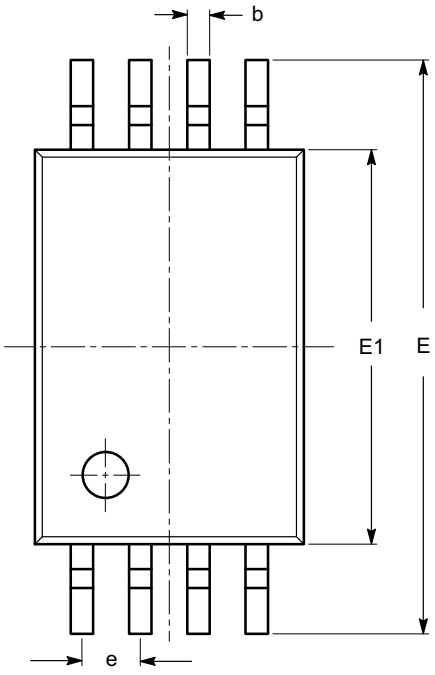
Table 7. AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit
f_{IN}	Input frequency	30	−	100	MHz
f_{OUT}	Output frequency	30	−	100	MHz
t_{LH} (Note 1)	Output rise time (measured at 0.8 V to 2.0 V)	0.7	0.9	1.1	nS
t_{HL} (Note 1)	Output fall time (measured at 2.0 V to 0.8 V)	0.6	0.8	1.0	nS
t_{JC}	Jitter (cycle−to−cycle)	−	−	360	pS
t_D	Output duty cycle	45	50	55	%

1. t_{LH} and t_{HL} are measured into a capacitive load of 15 pF

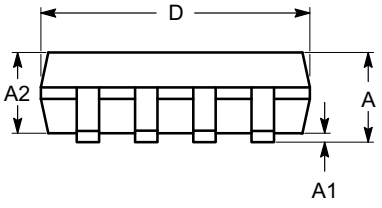
PACKAGE DIMENSIONS

TSSOP8, 4.4x3
CASE 948AL−01
ISSUE O

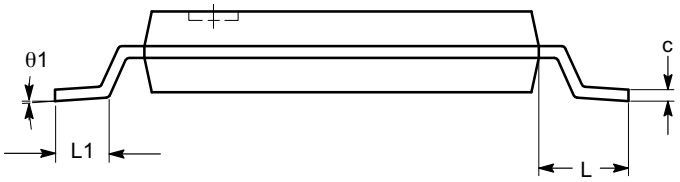


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80	0.90	1.05
b	0.19		0.30
c	0.09		0.20
D	2.90	3.00	3.10
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e	0.65 BSC		
L	1.00 REF		
L1	0.50	0.60	0.75
θ	0º		8º



SIDE VIEW



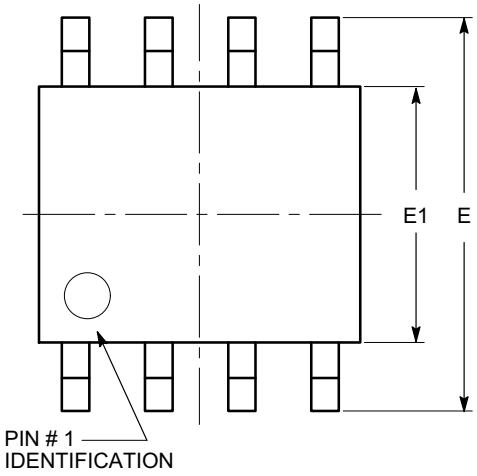
END VIEW

Notes:

(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-153.

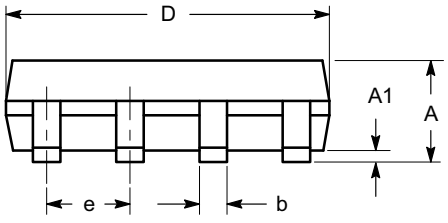
PACKAGE DIMENSIONS

SOIC 8, 150 mils
CASE 751BD−01
ISSUE O

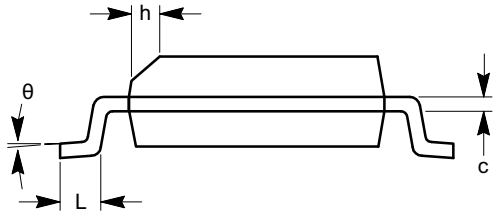


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e	1.27 BSC		
h	0.25		0.50
L	0.40		1.27
θ	0º		8º



SIDE VIEW



END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-012.

Table 8. ORDERING INFORMATION

Part Number	Marking	Package Type	Temperature
P2040AF−08−ST	P2040AF	8−Pin SOIC, Tube, Pb Free	Commercial
P2040AF−08−SR	P2040AF	8−Pin SOIC, Tape and Reel, Pb Free	Commercial
P2040AF−08−TT	P2040AF	8−Pin TSSOP, Tube, Pb Free	Commercial
P2040AF−08−TR	P2040AF	8−Pin TSSOP, Tape and Reel, Pb Free	Commercial
P2040AG−08−ST	P2040AG	8−Pin SOIC, Tube, Green	Commercial
P2040AG−08−SR	P2040AG	8−Pin SOIC, Tape and Reel, Green	Commercial
P2040AG−08−TT	P2040AG	8−Pin TSSOP, Tube, Green	Commercial
P2040AG−08−TR	P2040AG	8−Pin TSSOP, Tape and Reel, Green	Commercial
I2040AF−08−ST	I2040AF	8−Pin SOIC, Tube, Pb Free	Industrial
I2040AF−08−SR	I2040AF	8−Pin SOIC, Tape and Reel, Pb Free	Industrial
I2040AF−08−TT	I2040AF	8−Pin TSSOP, Tube, Pb Free	Industrial
I2040AF−08−TR	I2040AF	8−Pin TSSOP, Tape and Reel, Pb Free	Industrial
I2040AG−08−ST	I2040AG	8−Pin SOIC, Tube, Green	Industrial
I2040AG−08−SR	I2040AG	8−Pin SOIC, Tape and Reel, Green	Industrial
I2040AG−08−TT	I2040AG	8−Pin TSSOP, Tube, Green	Industrial
I2040AG−08−TR	I2040AG	8−Pin TSSOP, Tape and Reel, Green	Industrial
X2040AF−08−ST	I2040AF	8−Pin SOIC, Tube, Pb Free	Automotive
X2040AF−08−SR	I2040AF	8−Pin SOIC, Tape and Reel, Pb Free	Automotive
X2040AF−08−TT	I2040AF	8−Pin TSSOP, Tube, Pb Free	Automotive
X2040AF−08−TR	I2040AF	8−Pin TSSOP, Tape and Reel, Pb Free	Automotive
X2040AG−08−ST	I2040AG	8−Pin SOIC, Tube, Green	Automotive
X2040AG−08−SR	I2040AG	8−Pin SOIC, Tape and Reel, Green	Automotive
X2040AG−08−TT	I2040AG	8−Pin TSSOP, Tube, Green	Automotive
X2040AG−08−TR	I2040AG	8−Pin TSSOP, Tape and Reel, Green	Automotive

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P2040A/D